# APPLICATION NOTE

| | |
|---|---|
| **Product Name** | **EK-AI7688H**<br>**AI7688 IoT SiP Module** |
| **Version** | **A** |
| **Doc No** | **902-09004** |
| **Date** | **Dec 16th,2016** |



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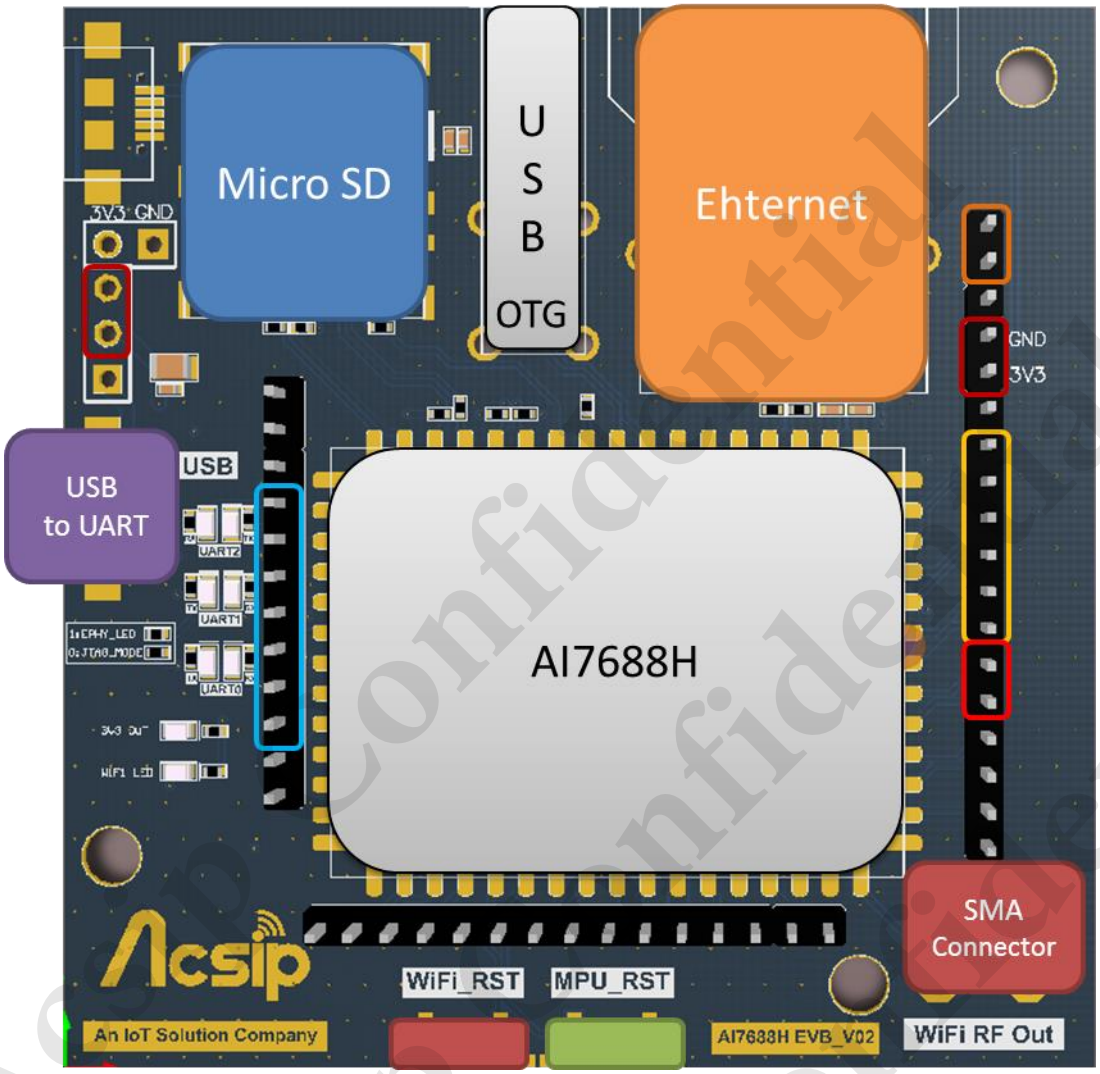
# Document History

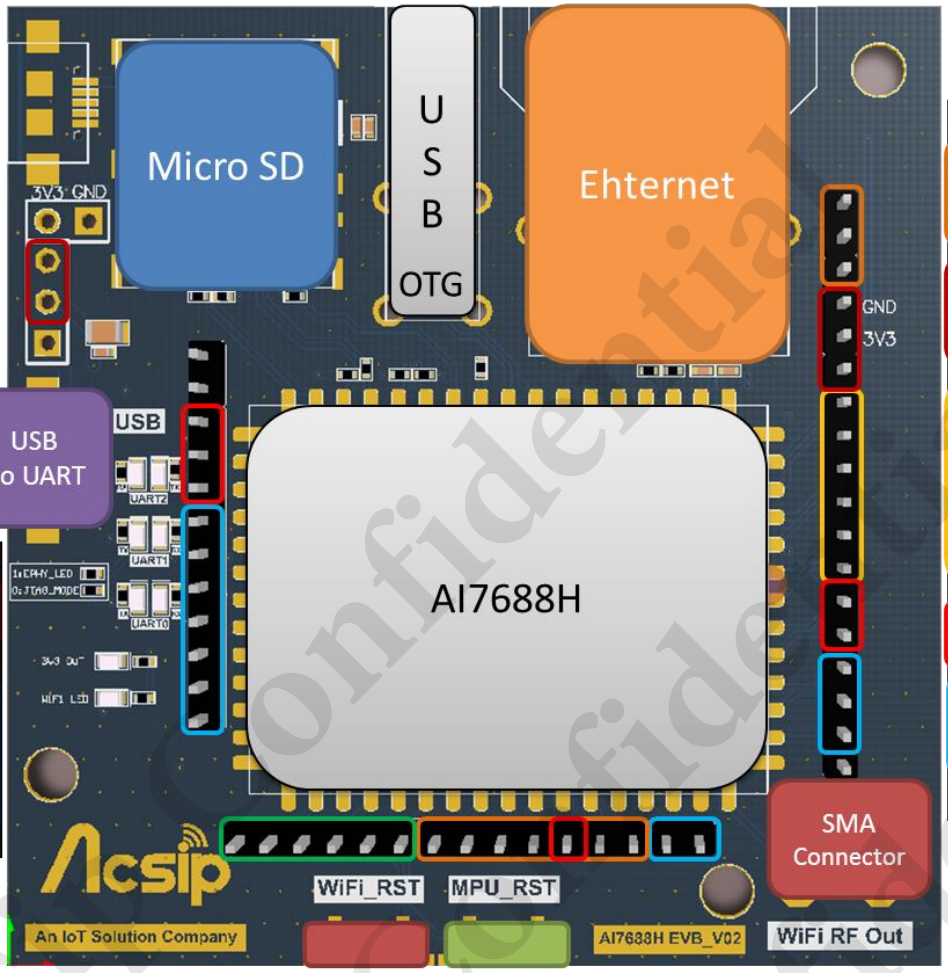
| Date | Revised Contents | Revised By | Version |
|---|---|---|---|
| Dec 16th,2016 | Initial release | Kevin | A |

# INDEX

# 1. Typical application



# 2. Pin Description




| Pin NAME | AI7688H_pinout |
|---|---|
| GND | 31 |
| UART_RXD2 | 32 |
| UART_TXD2 | 33 |
| MDI_RN_P2 | 34 |
| MDI_RP_P2 | 35 |
| MDI_RN_P1 | 36 |
| MDI_RP_P1 | 37 |
| MDI_TN_P1 | 38 |
| MDI_TP_P1 | 39 |
| GND | 40 |

| AI7688H_pinout | Pin NAME |
|---|---|
| 20 | UART_RXD0 |
| 19 | UART_TXD0 |
| 18 | GPIO0 |
| | GND |
| | 3V3 Out |
| | GND |
| 12 | I2C_SD |
| 11 | I2C_SCLK |
| 10 | I2S_CLK |
| 9 | I2S_WS |
| 8 | I2S_SDO |
| 7 | I2S_SDI |
| 6 | UART_RXD1 |
| 5 | UART_TXD1 |
| 4 | JTAG_RST_N |
| 3 | JTAG_TDO |
| 2 | JTAG_TMS |
| | GND |

| AI7688H_pinout | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin NAME | GND | WLED_N | REF_CLKO | PERST_N | WDT_RST_N | PORST_N | PCIE_TXP0 | PCIE_TXN0 | PCIE_RXP0 | PCIE_RXN0 | 3V3 | PCIE_CKN0 | PCIE_CKP0 | JCLK | JTDI |

| Module_pinout | Chip_pin_out | Pin NAME | Description |
|---|---|---|---|
| 1 | GND | | |
| 2 | 141 | EPHY_LED2 _N_JTMS | 10/100 PHY Port #2 activity LED, JTAG_TMS |
| 3 | 143 | EPHY_LED0 _N_JTDO | 10/100 PHY Port #0 activity LED, JTAG_TDO |
| 4 | 139 | EPHY_LED4_N_JTRST_N | 10/100 PHY Port #4 activity LED, JTAG_TRST_N |
| 5 | 147 | UART_TXD1 | UART1 Lite TXD |
| 6 | 148 | UART_RXD1 | UART1 Lite RXD |
| 7 | 16 | I2S_SDI | I2S data input |
| 8 | 17 | I2S_SDO | I2S data output |
| 9 | 18 | I2S_WS | I2S word select |
| 10 | 19 | I2S_CLK | I2S clock |
| 11 | 20 | I2C_SCLK | I2C Clock |
| 12 | 21 | I2C_SD | I2C Data |
| 13 | GND | | |
| 14 | 33 | MDI_RP_P0 | 10/100 PHY Port #0 RXN |
| 15 | 34 | MDI_RN_P0 | 10/100 PHY Port #0 RXP |
| 16 | 35 | MDI_TP_P0 | 10/100 PHY Port #0 TXN |
| 17 | 36 | MDI_TN_P0 | 10/100 PHY Port #0 TXP |
| 18 | 29 | GPIO0 | General Purpose I/O |
| 19 | 30 | UART_TXD0 | UART0 Lite TXD |
| 20 | 31 | UART_RXD0 | UART0 Lite RXD |
| 21 | 61 | USB_DP | USB Port0 data pin Data+ |
| 22 | 62 | USB_DM | USB Port0 data pin Data- |
| 23 | 49 | MDI_TP_P3 | 10/100 PHY Port #3 RXN |
| 24 | 50 | MDI_TN_P3 | 10/100 PHY Port #3 RXP |
| 25 | 51 | MDI_RP_P3 | 10/100 PHY Port #3 TXN |
| 26 | 52 | MDI_RN_P3 | 10/100 PHY Port #3 TXP |
| 27 | 54 | MDI_RP_P4 | 10/100 PHY Port #4 RXN |
| 28 | 55 | MDI_RN_P4 | 10/100 PHY Port #4 RXP |
| 29 | 56 | MDI_TP_P4 | 10/100 PHY Port #4 TXN |
| 30 | 57 | MDI_TN_P4 | 10/100 PHY Port #4 TXP |

| Module_pinout | Chip_pin_out | Pin NAME | Description |
|---|---|---|---|
| 31 | GND | | |
| 32 | 48 | MDI_TN_P2 | 10/100 PHY Port #2 TXP |
| 33 | 47 | MDI_TP_P2 | 10/100 PHY Port #2 TXN |
| 34 | 46 | MDI_RN_P2 | 10/100 PHY Port #2 RXP |
| 35 | 45 | MDI_RP_P2 | 10/100 PHY Port #2 RXN |
| 36 | 44 | MDI_RN_P1 | 10/100 PHY Port #1 TXP |
| 37 | 43 | MDI_RP_P1 | 10/100 PHY Port #1 TXN |
| 38 | 42 | MDI_TN_P1 | 10/100 PHY Port #1 RXP |
| 39 | 40 | MDI_TP_P1 | 10/100 PHY Port #1 RXN |
| 40 | GND | | |
| 41 | GND | | |
| 42 | GND | | |
| 43 | GND | | |
| 44 | GND | | |
| 45 | 144 | WLED_N | WLAN Activity LED |
| 46 | 136 | REF_CLKO | Reference Clock Ouptut |
| 47 | 135 | PERST_N | PCIe device reset |
| 48 | 137 | WDT_RST_N | Watchdog timeout reset |
| 49 | 138 | PORST_N | Power on reset |
| 50 | 127 | PCIE_TXP | PCIe0 differential transmit TX + |
| 51 | 126 | PCIE_TXN0 | PCIe0 differential transmit TX - |
| 52 | 129 | PCIE_RXP0 | PCIe0 differential receiver RX + |
| 53 | 130 | PCIE_RXN0 | PCIe0 differential receiver RX - |
| 54 | 3.3V | | |
| 55 | 132 | PCIE_CKN0 | External reference clock output (negative) |
| 56 | 133 | PCIE_CKP0 | External reference clock output (positive) |
| 57 | 140 | EPHY_LED3 _N_JTCLK | 10/100 PHY Port #3 activity LED, JTAG_CLK |
| 58 | 142 | EPHY_LED1 _N_JTDI | 10/100 PHY Port #1 activity LED, JTAG_TDI |
| 59 | GND | | |
| 60 | RF | | |

# 3. Hardware Guide

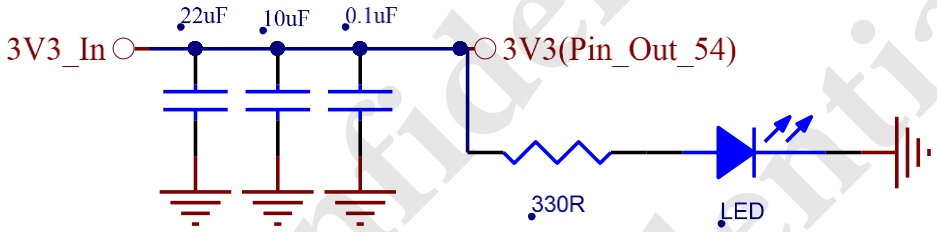
## 3-1. RF Layout(Pin_Out_60)

CPWG-type traces used for RF function are recommended, which having better EMC and RF capability.

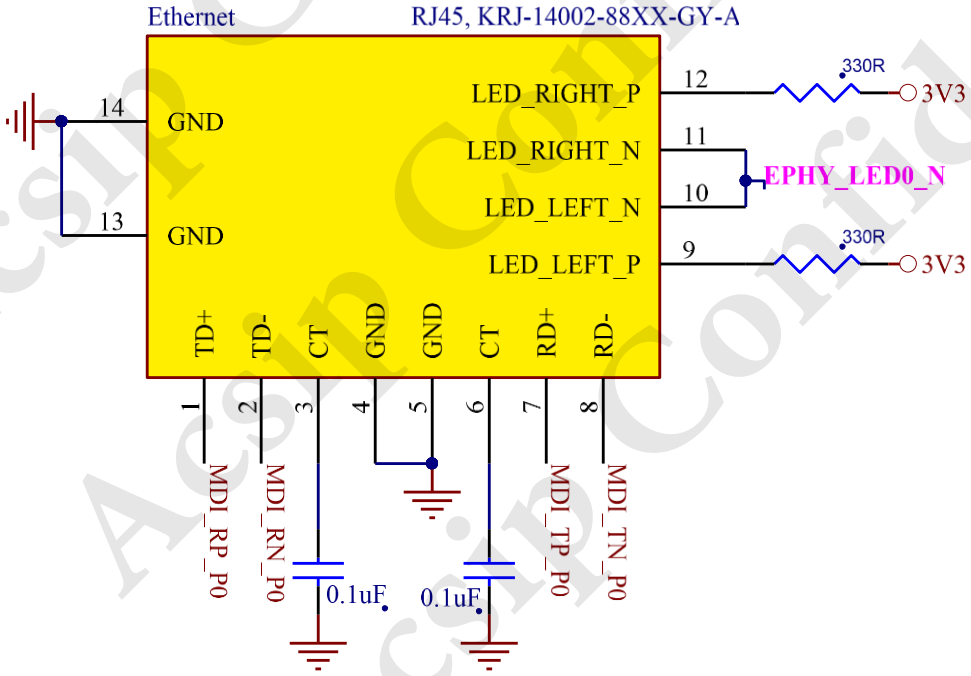
Note: Suggest reserving matching circuit between module and Antenna.

## 3-2. DC Power

The 3V3 power trace width should be >=40mil




## 3-3. Ethernet Schematic




•Separate each Ethernet pairs with “well GND shielding”

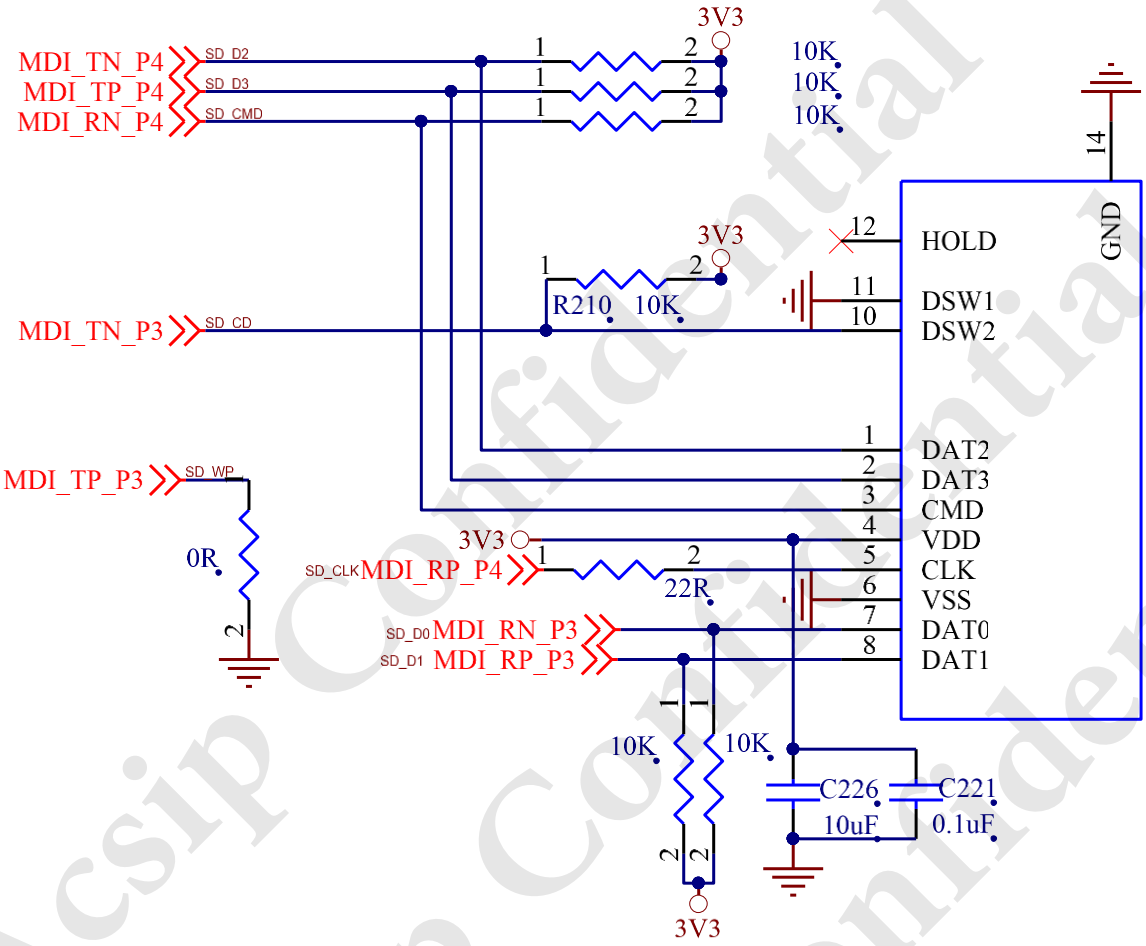
•Impedance is 100-ohm (differential)

•With >80mil gap between ethernet GND plane & system GND plane

•Ethernet pair between transformer & RJ-45 connector should meet width/space=18/5mil

## 3-1.SD Schematic

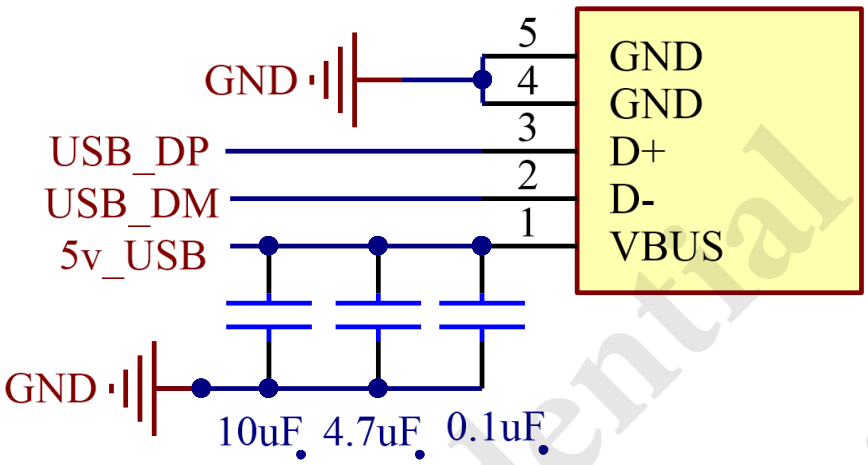
**Please make sure the selected SD tray behavior is matching the table shown as below, in order to keep SD functionality.**




| SWITCH | WITHOUT CARD | WITH CARD |
|---|---|---|
| | DSW1 DSW2 ④ ⑤ ⑥ GND GND SD_CD Pull Low | DSW1 DSW2 ④ ⑤ ⑥ GND GND SD_CD Pull high |

| | | CONTACT AREA | TERMINAL AREA |
|---|---|---|---|
| ① | CONTACT | Au (0.5μm MIN) OVER Ni (2μm MIN) | Au FLASH (0.03μm MIN) OVER Ni (1μm MIN) |
| ⑤ | DETECTION SWITCH 1(DSW1) | Au (0.1μm MIN) OVER Ni (1μm MIN) | |
| ⑥ | DETECTION SWITCH 2(DSW2) | | |
| ④ | TOP COVER | - | Au FLASH (0.03μm MIN) |

## 3-4. USB Schematic

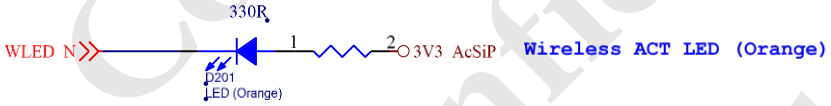



•Keep USB_DP / DM differential pairs routing with well “GND shielding”

•Impedance is 90-ohm (differential)

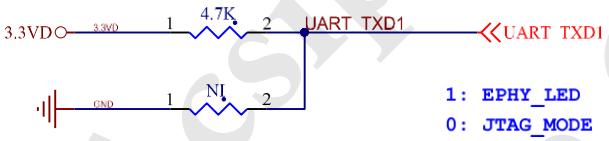
•USB_5V power trace >=20mil

## 3-5. LED Schematic




## 3-6. Other Schematic

•JTAG MODE




•MPU Reset / WIFI Reset